

Define intermediate states that initial sequence of bits is to be transformed into

Define control configuration bits for transforming initial sequence into intermediate states

FIG. 2

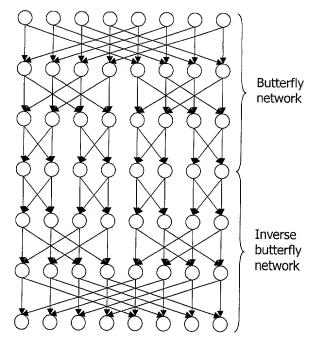


FIG. 3A

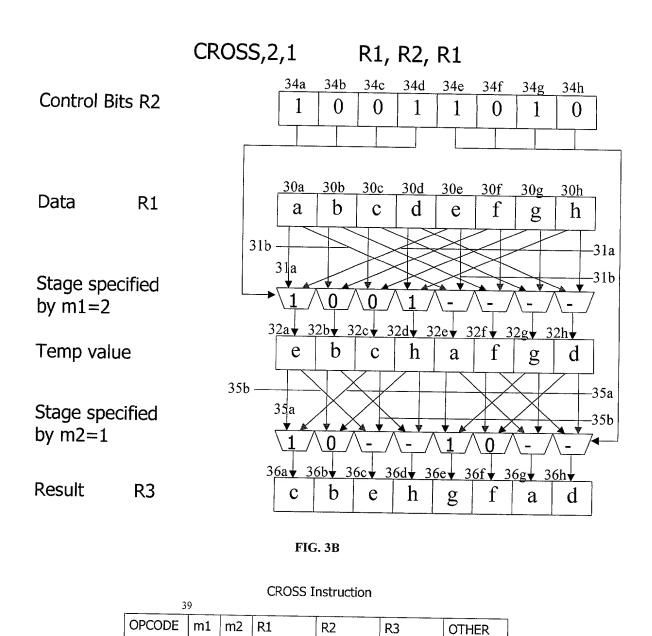


FIG. 3C

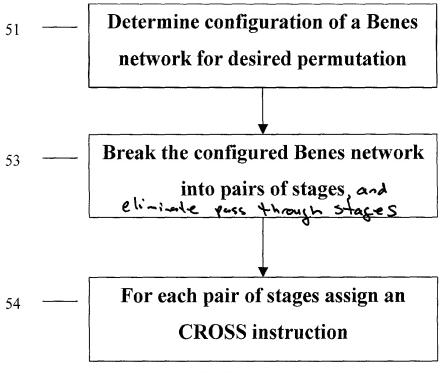


FIG. 4A

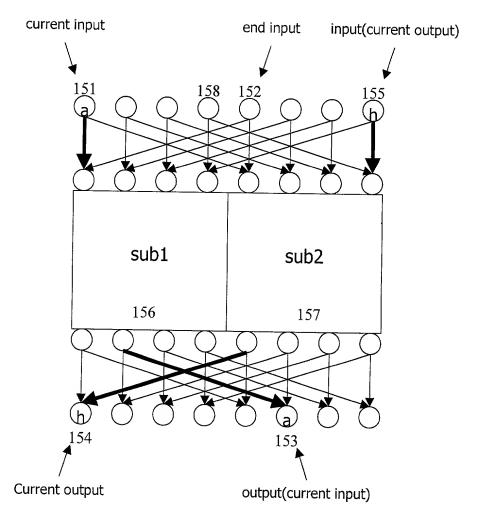


FIG. 4B

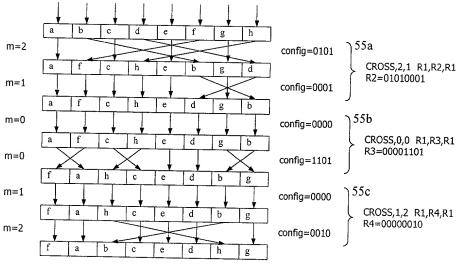
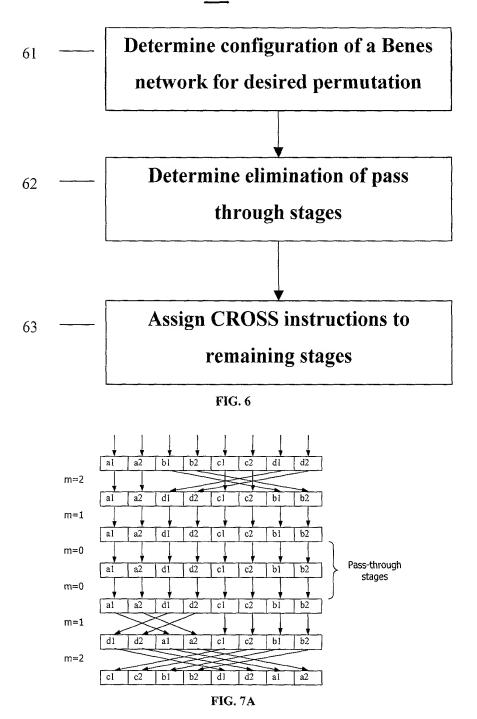
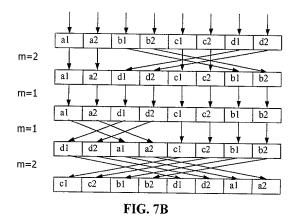
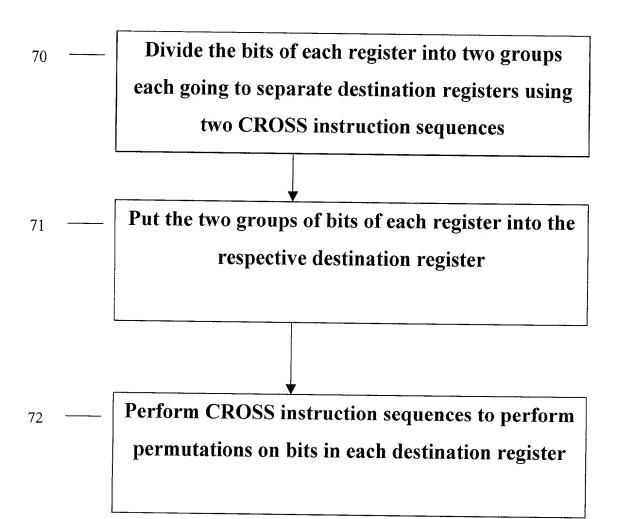
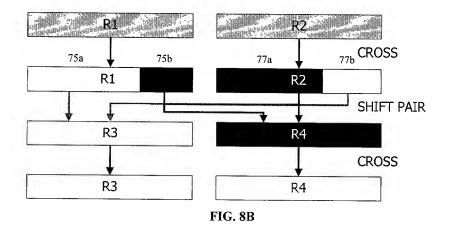


FIG. 5









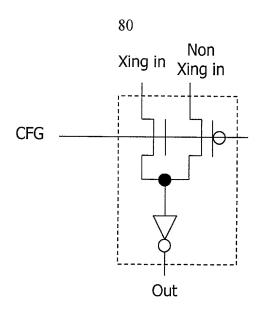


FIG. 9A

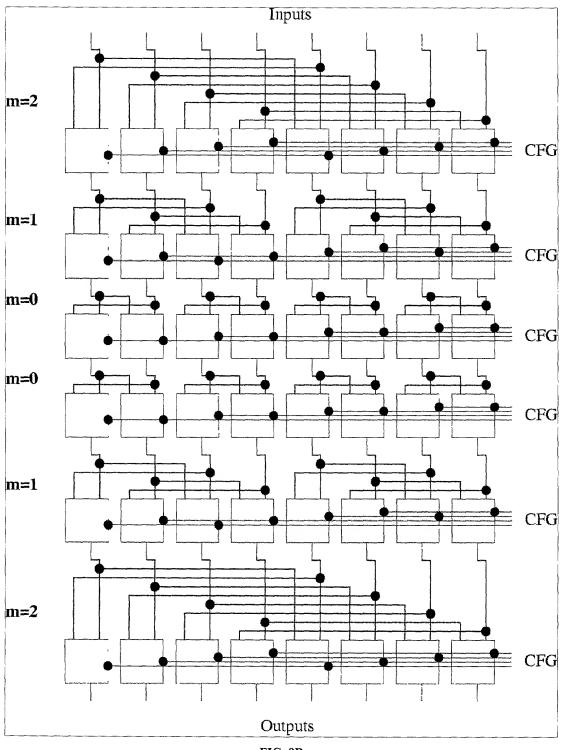
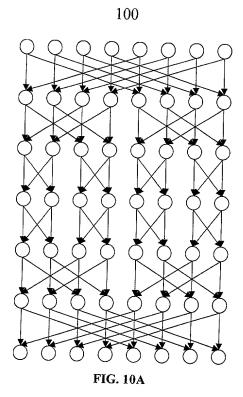
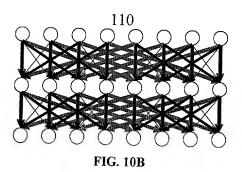


FIG. 9B





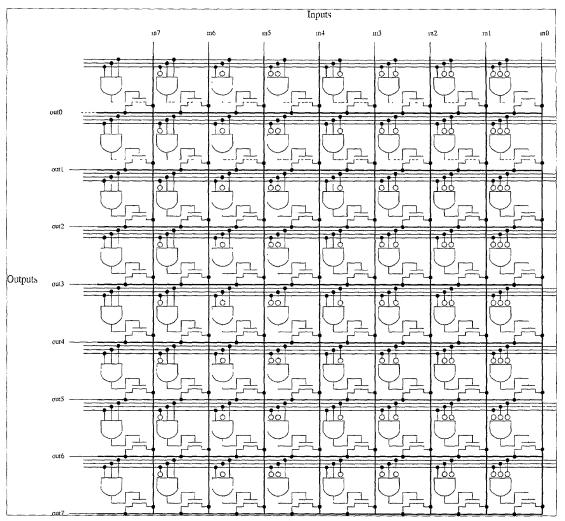


FIG. 11

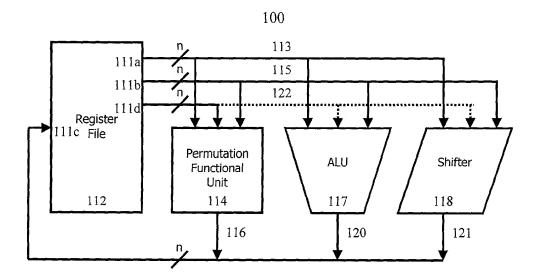


FIG. 12A

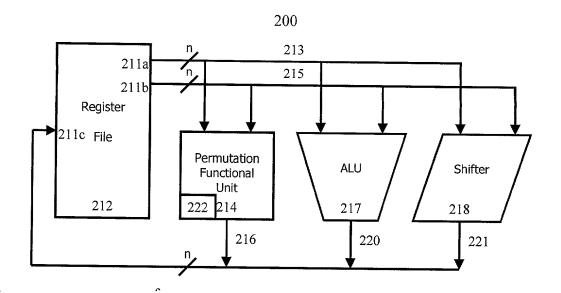


FIG. 12B